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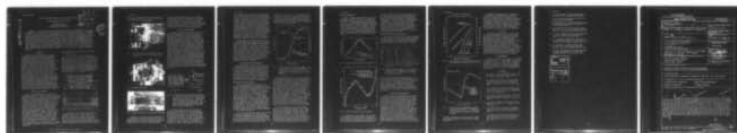
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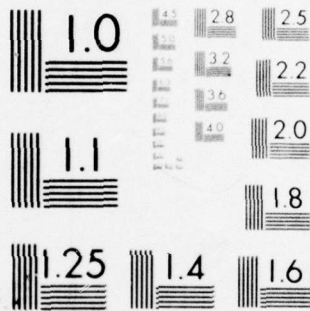
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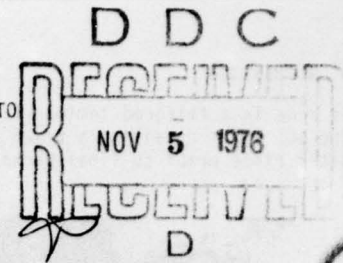


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STABLE CW OPERATION OF GAP-COUPLED SILICON-ON-SAPPHIRE TO
 LiNbO_3 ACOUSTOELECTRIC AMPLIFIERS*

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ABSTRACT: Technological advances are detailed which improve the performance of gap-coupled acoustoelectric amplifiers for dc drift field operation. The amplifier configuration is a segmented 1- μm thick layer of 20 Ωcm n-type silicon-on-sapphire held in close proximity to a 21- μs (YZ) LiNbO_3 delay line. The combination of ion-beam-etched spacer posts on the delay line surface and a simple packaging scheme utilizing the sapphire wafer as a pressurized diaphragm allow reproducible formation of uniform air-gaps of the order of 0.1 μm over a 1.5 mm x 2.5 cm area. Transverse dc fringing fields are effectively terminated both at the surface traps of the chemically-stripped and depleted Si surface and at the deep acceptor-donor pair traps within the Si film. Thus the electron-sheet homogeneity is preserved even at drift fields over 2 kV/cm and the theoretical S-shaped gain characteristic is observed. For an effective coupling gap of 0.17 μm a typical 1/2-cm long segment has peak electronic gain of over 21 dB at 140 MHz with a minimum acoustic noise figure of 7 dB near 1 kV bias. Intermodulation distortion products are more than 50 dB below signal for output sheet powers under 2 dBm/mm. Phase deviation relative to the delay line alone is only 0.7° rms for 4 cascaded segments.

Introduction

There exists a well-recognized need in real-time signal processing systems for long, wideband, nondispersive delay lines of wide dynamic range. The ideal solution for SAW lines is to preserve signal strength by providing noise-free amplification continuously and uniformly throughout the delay period, in which case the dynamic range achievable is that of a lossless line. A practical implementation of this concept would employ acoustoelectric amplifiers internal to the delay line, and initial efforts to develop such devices received much attention. But the inability to fabricate, reproducibly, any device exhibiting stable terminal gain with low noise figure for dc drift field operation near room temperature has prevented system applications. At present, long delay lines of wide dynamic range must be pieced together from shorter crystals with external interstage electronic amplification, and thus suffer loss and bandwidth compression with each transduction. This paper reports technological advances which improve acoustoelectric amplifier performance to the point of reproducible CW operation, thereby bringing closer to system realization the concomitant benefits of long delay capacity, wide bandwidth, echo suppression, isolation of adjacent taps, and wide dynamic range.

Amplifier Configuration

Three possible SAW amplifier configurations are available: the monolithic type¹, the air-gap type², and the deposited-film³. The ability for the independent optimization of material parameters and the separate processing of semiconductor and piezoelectric components is inherent to the gap-coupled structure. This flexibility, combined with the facts that a technology exists to make spacer posts by ion-beam etching the piezoelectric crystal surface^{4,5} and that high-quality convolver performance of such structures has been demonstrated⁶, makes the air-gap approach the one with the lowest developmental risk. Preliminary dc operation of gap amplifiers using a Si epitaxial film on a sapphire substrate⁷, a depletion layer in bulk GaAs bonded to sapphire⁸, and an accumulation layer in bulk Si⁹ have been reported. All results underscored the obvious thermal constraint that the conducting layer within the semiconductor be of the order of the Debye length for efficient dc operation. For the work reported here commercially available

silicon-on-sapphire (SOS) wafers and (YZ) LiNbO_3 crystals were chosen.

A cross-sectional view of the amplifier is shown in Fig. 1. As in convolver⁶ and memory-correlator¹⁰ devices reported in this session, the desired gap-height is established by means of ion-beam etched posts approximately 4- μm square in a pseudo-random array with average row spacing of about 200 μm . The novel feature of this package is the use of the SOS wafer as a pressurized diaphragm to establish uniform coupling over the 0.1-cm x 2.0-cm interaction region. The delay line rests on a molded silicone gel which enables the top LiNbO_3 surface to become parallel to the Si film as pressure is applied.

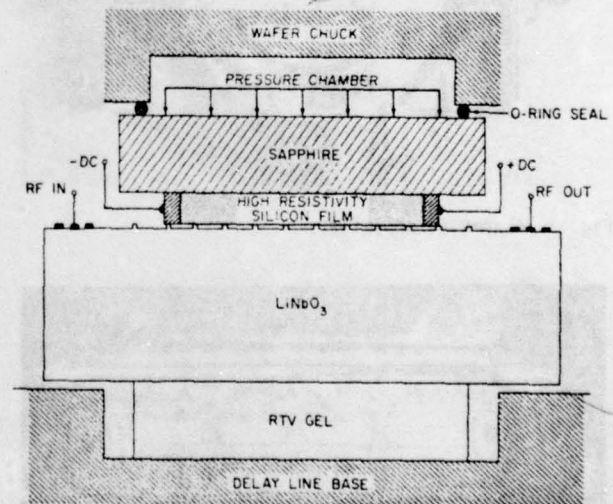


Fig. 1 Cross-section view of the amplifier.

Photographs of a device before and after final assembly are shown in Fig. 2 and 3 respectively. Standard microelectronic techniques were used to fabricate four amplifier segments on each sapphire disk. The drift field is established through n^+ contact bars which have Cr/Au-metallized end pads to contact the Au-plated spring-loaded probes incorporated into the rectangular Plexiglas crystal-holder. Assembly

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is done in a filtered laminar-flow air bench, with the SOS wafer receiving a brief buffered-HF etch and water rinse prior to final packaging.

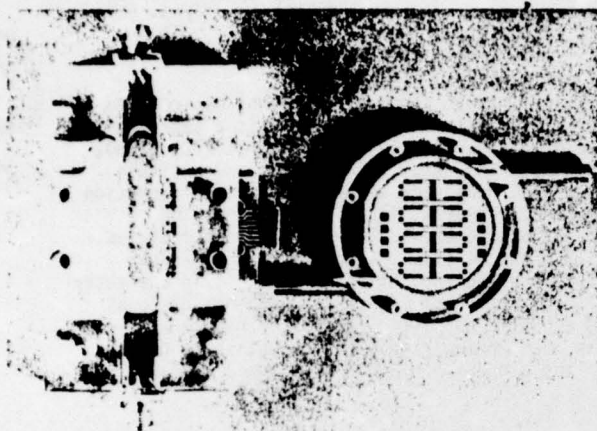


Fig. 2 Amplifier prior to final assembly. The SOS wafer is 1.5-in dia., 0.013-in thick, with 1- μ m Si film.

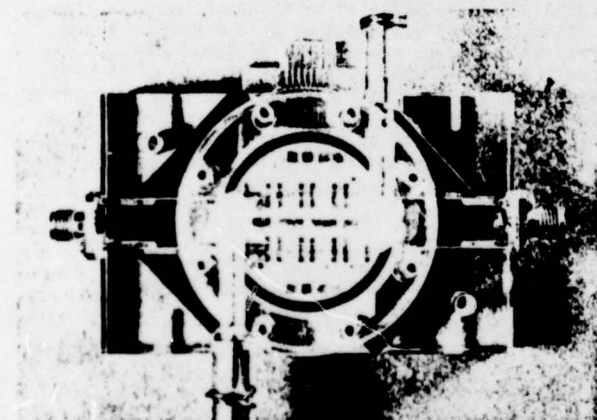


Fig. 3 Assembled amplifier.

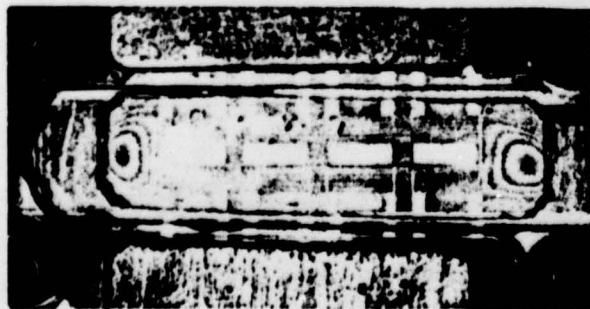


Fig. 4 Typical interaction region with 0.13- μ m air gap.

Figure 4 is a close-up of the interaction region as viewed through the silicone gel and delay line. A modest pressure of 3-10 psi is sufficient to establish the desired gap. While the unloaded post-height is nominally 0.2 μ m for this delay line, both inter-

ference fringes and the acoustoelectric interaction indicate that the posts have deformed so as to yield a uniform gap near 0.13 μ m. Gaps of this height are easily and reproducibly achieved over the entire interaction region. Achieving uniform gaps below 0.1 μ m over the entire area is made difficult by post deformation and is troublesome with the present plastic-package/slender-post/thick-sapphire configuration.

Design Considerations

A viable acoustoelectric amplifier must not only operate with dc drift field, it must maintain an essentially homogeneous sheet of free carriers, for only then will the maximum gain and minimum noise performance be realized. Figure 5a represents the rf interaction between drifting electrons in the Si and the charges induced in the LiNbO_3 . A simple calculation indicates that the condition for achieving maximum gain requires a drift field comparable to the normal electric field that the assumed charge sheet would itself produce¹¹. Hence near the contacts, where the normal component of the fringing drift field is high, the electron density may be modified substantially. Indeed, the pulsed and dc results on earlier Si devices indicated a depletion of mobile carriers near the anode (SAW receiver). The achievement of maximum gain requires that the product of sheet density and drift velocity be constant, hence in an inhomogeneous amplifier the conditions for peak gain cannot be simultaneously achieved throughout the device. The gain of earlier experimental amplifiers at elevated dc fields fell substantially below that expected. Although no noise measurements were reported for dc operation, it is expected that the amplifier noise figure was degraded due to the existence of highest gain near the receiving transducer.

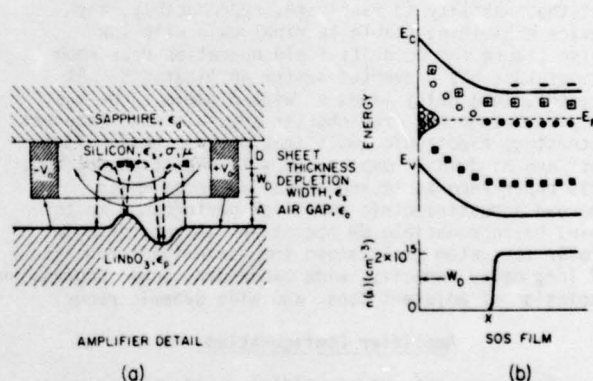


Fig. 5 (a) Acoustoelectric bunching of electrons by rf fields (dashed arrows) in presence of fringing drift field (solid arrows). Typical device has $D=W_D=0.5 \mu\text{m}$, $A=0.13 \mu\text{m}$. (b) Energy band diagram and charge distribution of SOS film versus distance from stripped surface. The forbidden gap contains phosphorous donors (\square), charged surface states (\ominus), and deep donor (\blacksquare) and acceptor (\bullet) traps.

Accumulation-mode devices, with the electron sheet at the semiconductor surface, were especially susceptible to fringing fields. The results reported here indicate that commercially available SOS, when suitably processed, serves to shield mobile carriers from transverse dc fields. Figure 5b is a schematic representation of the energy bands and charge concentration within a typical SOS layer. The surface is stripped of all oxide, and thus the high density of acceptor-like (negative when occupied) surface states

pins the Fermi level at about 1/3 of the forbidden gap. For the $2 \times 10^{15} \text{ cm}^{-3}$ donor density of the SOS used in the best devices, this surface charge should result in a depletion width of 0.56 μm , about 1/2 the epilayer. The Si layer is also known to contain a high density of deep traps caused by lattice misfit at the Si-Al₂O₃ interface and the resultant propagation of crystalline imperfections. These levels have been described¹² as a donor level located about 0.3 eV from the valence band edge and an acceptor level located about 0.25 eV from the conduction band edge. The donor-acceptor pair occur in approximately equal densities of up to 10^{18} cm^{-3} and have an energy spread of over 0.1 eV. No attempt has been made to model the Si-Al₂O₃ interface, as it is shielded from the acoustoelectric interaction for practical device parameters. Probably the Fermi level is pinned near the substrate where the trap densities are highest.

The existence of these deep levels, both at the surface and distributed throughout the layer, serve as possible charge sites to terminate normal electric fields and prevent gross distortion of the carrier sheet. The tradeoff to obtain this low-frequency shielding is that some of the traps are sufficiently near the Fermi level to respond to the rf fields and thereby reduce the desired gain mechanism. Also, this fast portion of the traps can be the predominant noise mechanism. Another, obvious tradeoff, is that the drift mobility in SOS is only 50-70% of that found in comparably doped bulk Si and hence higher fields are required to achieve peak gain. The remainder of this paper serves to illustrate the appropriateness of such tradeoffs.

Continuous Drift Field Operation

The most extensive data was obtained on a series of segmented amplifiers fabricated with n-type SOS material with as-purchased phosphorous densities of $2 \times 10^{15} \text{ cm}^{-3}$ in 1.0- μm thickness (nominal $2 \times 10^5 \Omega/\text{square}$). Also tested were 0.6- μm and 1.0- μm thick films with 8×10^{14} donors/ cm^3 . The thinner films were found to be fully depleted when stripped, the others were mated to 21- μs delay lines with nominal post heights of 0.05-, 0.1-, and 0.2- μm . All of the data which follow pertain to the 1.0- μm thick, 2×10^{15} donors/ cm^3 , 0.2- μm -high post configuration.

Amplifier Gain and Noise Figure

The experimental 140 MHz internal gain and internal noise characteristics as functions of drift voltage for a single 0.5-cm long segment are indicated in Fig. 6. Synchronism is observed at 0.22 kV, implying an effective drift mobility of nearly 800 cm^2/Vs . Peak gain of over 21 dB is achieved at 1.05 kV, thus terminal gain is realized with a single section. The actual air-gap for this device and those following is near 0.13 μm , to which must be added the approximate 0.04 μm electrical width of the depletion layer, for an effective coupling gap near 0.17 μm . The gain curve is observed to match, even at high voltage, the familiar S-shaped characteristic calculated from the full expressions developed by Kino and Reeder¹³. Best fit was obtained for a sheet resistivity of $4 \times 10^5 \Omega/\text{square}$, a value in good agreement with both the $4.7 \times 10^5 \Omega/\text{square}$ measured at dc and the approximate $4.5 \times 10^5 \Omega/\text{square}$ expected for the partially depleted film.

This is the first amplifier configuration reported with stable dc operation in which the maximum excursions of the homogeneous-sheet gain characteristic are obtained. Uniformity of single-segment characteristics is excellent both intra and inter wafer. The spread among four segments on a typical wafer was $\pm 0.01 \text{ dB/V}$ in gain slope at synchronism and $\pm 1.2 \text{ dB}$ in

maximum gain. Most of this variation correlates with differences in terminal conductance and may be attributed to minor variations in dopant and trap densities. Electronic gain was characterized at the transducer fundamental (140 MHz) and harmonic (410 MHz) frequencies for the three post heights, and in general the amplifier behavior scaled as expected.

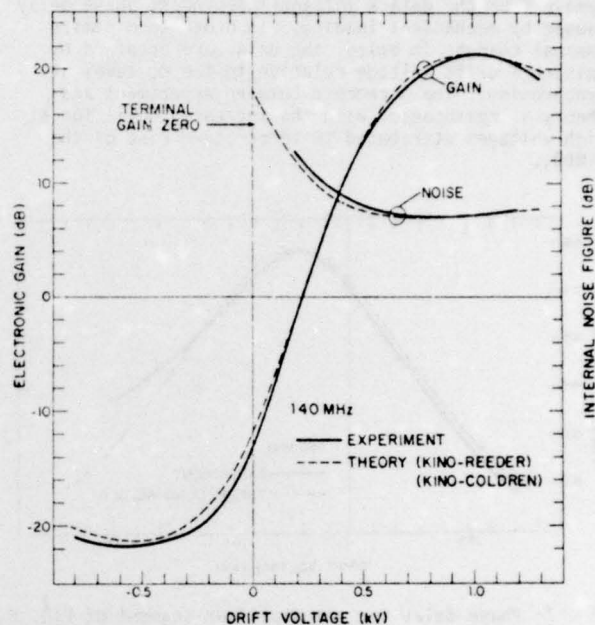


Fig. 6 Internal gain and internal noise figure versus voltage for a 5-mm long amplifier segment. Theoretical performance is calculated for the parameters $A = 0.13 \mu\text{m}$, $W_D = 0.56 \mu\text{m}$, $\mu = 800 \text{ cm}^2/\text{Vs}$, $\rho/D = 4 \times 10^5 \Omega/\text{square}$, 10% electrons trapped.

The noise behavior of Fig. 6 is the first reported for dc operation. Acoustic noise has been plotted. Thus for terminal characteristics one need account for propagation and transduction losses, and the gain and noise of additional amplifier segments. The noise is observed to decrease initially with applied voltage, pass through a broad minimum of 7 dB in the region of maximum gain near 0.8 kV, then slowly rise again. Such behavior has been treated by Kino and Coldren¹⁴, who indicate that fast traps are the major noise source in actual devices. The noise performance seen here is closely matched by their model with 90% of the mobile carriers remaining untrapped. In an idealized device with no fast traps, a noise figure of only 2.5 dB would be obtained at 0.8 kV. The 7 dB minimum obtained here represents an improvement over the 11 dB figure reported¹⁴ for a pulsed SOS amplifier with twice the trap density. A somewhat better noise figure of 5.5 dB was observed¹⁵ for a pulsed accumulation layer device in bulk Si having low trap density.

A suitable operating point for the prototype amplifier is 0.8 kV, where 20 dB gain and 7 dB added noise figure per segment are obtained. The dc power dissipated as Joule heating within the acoustic beam width is 0.27 W per segment. Complete wafers have been operated with up to 2.5 W of total dc input. Generally a low flow (5 scfh) of room temperature N₂ was employed to provide a stable pressure against the SOS diaphragm and to afford some cooling. With such minimal cooling, the thermal transient produced by a 1-kV step in drift voltage lasted up to 10 minutes.

Amplifier Phase Delay

Figure 7 indicates the phase delay in cycles for the amplifier segment of Fig. 6. As expected, the maximum delay occurs at synchronism. Included for comparison is the appropriate Kino-Reeder prediction. The curves have been matched at the peak in order to remove from the data a voltage-independent phase delay caused by mechanical loading. In order to minimize thermal changes in delay, the data were obtained by pulsing a drift voltage relative to the dc level at synchronism. The agreement between experiment and theory is reasonable, with the increased deviation at high voltages attributed to temperature rise of the LiNbO_3 .

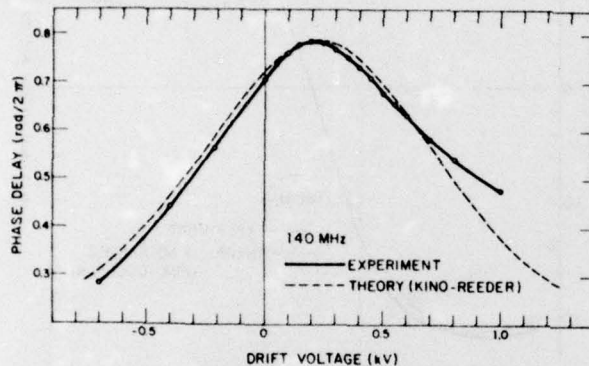


Fig. 7 Phase delay for the amplifier segment of Fig. 6.

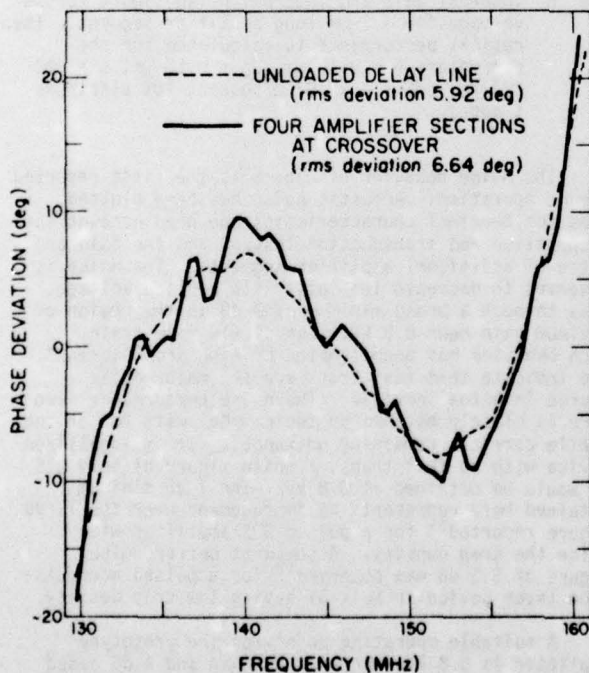


Fig. 8 Linear phase deviation versus frequency.

The dispersion of a gap-coupled structure must be minimized for a practical device. As is seen in Fig. 8, the phase characteristic of the amplifier is essentially linear, with the major deviation over the 130 to 160 MHz band contributed by the transducers.

The delay line alone has a 5.92° rms deviation. When all four segments are operated at synchronism for peak delay, the device shows a 6.64° rms deviation, hence the 2-cm interaction length has added only 0.7° rms deviation. The fine structure in the phase data is attributed to spurious reflections which occur within the diffused contacts at each end of the segments. These regions are about $175\text{-}\mu\text{m}$ long and, due to the removal of diffusion glass, lie about $0.3\text{ }\mu\text{m}$ below the undoped Si surface. By a combination of electrical and mechanical discontinuities these regions form a family of acoustic cavities, each with resonances spaced by about 9 MHz.

Distortion, Saturation, and Efficiency

The dynamic range over which the amplifier transfer function is essentially linear can be easily determined by a two-tone test. Typical spectrum analyzer traces of device output are indicated in Figs. 9a and 9b for low and high signal levels respectively. Complete

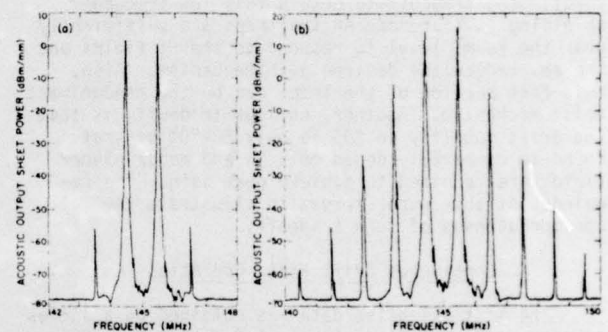


Fig. 9 Spectrum analyzer traces of 144.5 + 145.5 two-tone test for four segments with 30 dB total electronic gain. (a) Amplifier unsaturated (b) Amplifier saturated.

results for the four segment unit operating at 1.3 times synchronism with 30 dB electronic gain are in Fig. 10. The acoustic sheet power at which 1-dB gain compression occurs is 12 dBm/mm at the output. With output sheet power below 2 dBm/mm, the distortion products are more than 50 dB below the signal. An approximate efficiency of about 1% for a practical amplifier segment can be estimated for operation with 20 dB gain, 7 dB noise figure, and distortion products 50 dB down.

Future Design Considerations

Two relatively minor complications in the present configuration involved spurious reflections within the amplifier contacts and deformation of the spacer posts. Both can be solved with moderate design effort. One troublesome, but not unexpected, feature of the present devices became apparent after several weeks of evaluation. Initially homogeneous amplifiers were observed to increase in terminal resistance and exhibit gain characteristics indicative of carrier inhomogeneity. Figure 11 indicates the gain characteristic obtained more than one month after stripping and assembly. Terminal dc resistance has increased, and the peak gain has dropped. These are the effects to be expected of carrier inhomogeneity, as can be qualitatively illustrated by choosing a convenient model¹¹ of linearly decreasing electron density between cathode and anode and integrating the spatially varying incremental gain along the device length to obtain the terminal characteristics. Figure 11 includes

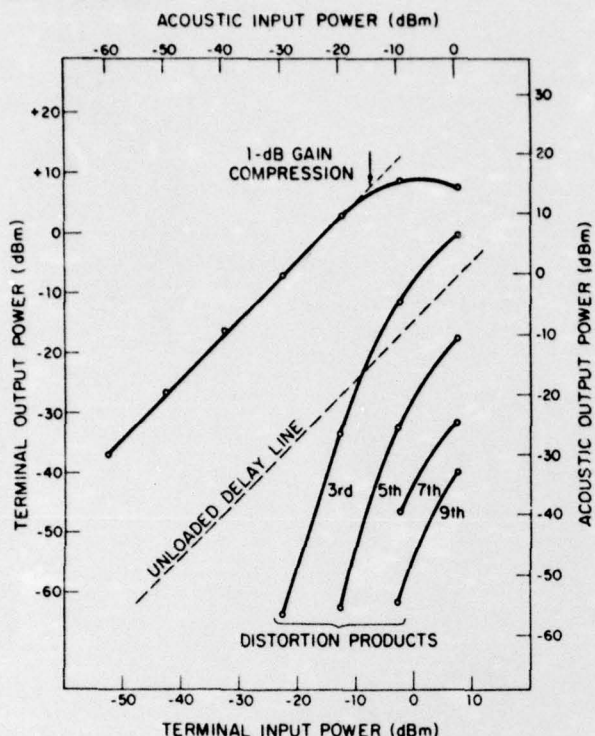


Fig. 10 Gain saturation and distortion product generation characteristics for amplifier of Fig. 9.

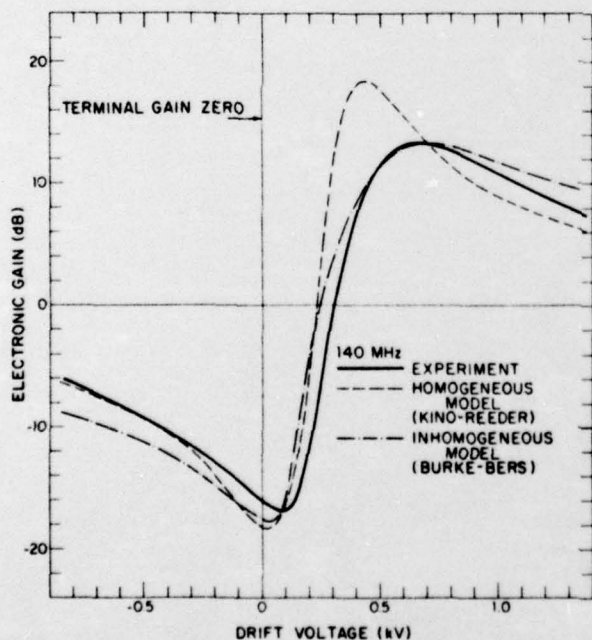


Fig. 11 Effect of electron inhomogeneity on gain of single amplifier segment. All parameters as in Fig. 6 except $\rho/D = 1.75 \times 10^6 \Omega/\text{square}$, electron density at cathode 4.7 times that at anode.

the model predictions for both no carrier variation and for a concentration 4.7 times higher at cathode than anode.

Degradation occurs because the Si surface has slowly formed, at room temperature, an oxide which serves to annihilate many of the surface states present on a stripped surface. Apparently the electrons are not sufficiently screened from fringing fields by the deep donor-acceptor pair alone and the amplifier performance is limited by inhomogeneities. Alteration of the amplifiers might be prevented by simply sealing them in a hermetic package. Another approach would be to permanently pin the Si surface by creating a high density of surface states with ion implantation.

Conclusions

Long wideband SAW delay lines with good dynamic range would find application within many real-time signal processing systems. Compensation of Rayleigh wave attenuation by distributed acoustoelectric amplification has several attractive features. In the VHF and lower UHF ranges, gap-coupled configurations do not impose a severe limitation on amplifier performance. The device performance reported here indicates that available materials quality and fabrication technology favor air-gap devices. The demonstration of reproducible, well-behaved, continuously operating homogeneous amplification with reasonable noise figure by using commercially available materials and well known fabrication techniques renews the promise that practical systems applications are feasible.

Acknowledgements

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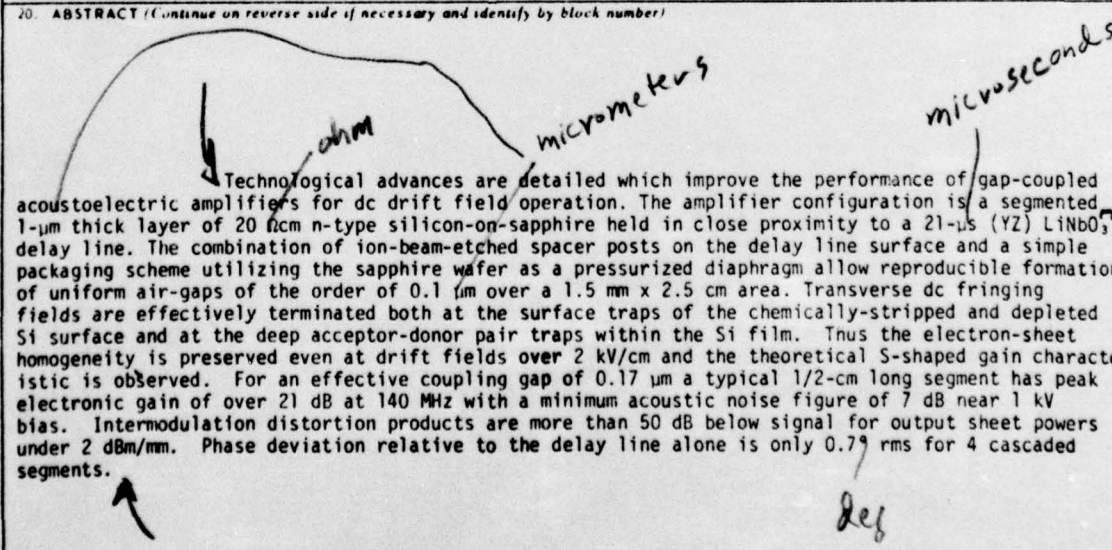
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